REMARKS

Claims 1-42 are pending. Claim 37 has been amended, without acquiescence or prejudice to pursue in a related application. The support for the amendments can be found at least in paragraphs 44 and 45 of the originally filed specification. No new matter has been added.

Allowable Subject Matter

Applicants would like to thank the Examiner for indicating claims 3-5, 10-13, 15-17, 22-24, 29-32 and 34-36 include allowable subject matter. However, Applicants note that claims 15-17 were also rejected by the Office action under 35 U.S.C. §102(e). Clarification is requested.

Claim Rejections Under 35 U.S.C. §101

Claims 37, 41 and 42 were rejected under 35 U.S.C. §101 because the claimed invention in these claims are allegedly directed to non-statutory subject matter. Applicants respectfully traverse. Claim 37 has been amended without prejudice. Thus, the rejection to claims 37, 41 and 42 is now moot. Withdrawal of this rejection is respectfully solicited.

Claim Rejections Under 35 U.S.C. §102(e)

Claims 1, 2, 6-9, 14-17, 21, 25-26 and 37-38 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Srinivasan et al. (US 7,076,758 B1).

Claim 1 explicitly recites the feature of "conducting signal integrity optimization in conjunction with detailed routing of the integrated circuit design based upon the global routing plan, wherein the detailed routing is performed on spacing made available for routing allocated based on a priority determined by the signal integrity optimization" (emphasis added). Srinivasan et al. does not disclose at least this claimed feature.

Srinivasan is directed to using router feedback for placement improvement for logic design. Srinivasan et al. discloses a method of physical circuit design including assigning initial locations to components in the circuit design and determining an initial routing of connections

between components in the circuit design using an overlap mode. The method also can include determining timing critical connections and selectively relocating components with at least one timing critical connection prior to performing a detailed routing of the circuit design.

The Office action incorrectly states that Figs. 1-2; route signals in delay mode and resource mode discloses all the limitations of the claims. Srinivasan et al. does not disclose at least signal integrity optimization as claimed.

Specifically, Srinivasan et al. discloses routing in resource and delay modes. Optimizing connections in resource (shortest amount of wires) or delay (minimal propagation delay) modes of Srinivasan et al. is not the same as signal integrity optimization as claimed. Signal integrity represents issues relating to the sources of noise and/or noise level in an integrated circuit design and their effect on performance. Routing with respect to shortest amount of wires or minimizing propagation delay is not the same as optimizing with respect to issues relation to sources of noise and/or noise level. In fact, Srinivasan et al. does not consider and is silent with respect to noise. Thus, Srinivasan et al. does not teach or suggest the feature of "conducting signal integrity optimization in conjunction with detailed routing of the integrated circuit design based upon the global routing plan, wherein the detailed routing is performed on spacing made available for routing allocated based on a priority determined by the signal integrity optimization" (emphasis added).

In addition, claims 2, 6-9, 14-17, 21, 25-26 and 37-38 also include at least this limitation. Therefore, these claims are also not anticipated by Srinivasan et al. for at least the same reason.

Claim Rejections Under 35 U.S.C. §103

Claims 18-20 were rejected under 35 U.S.C. §103(a) as unpatentable over Srinivasan et al. in view of Igusa et al. (US 6,782,520). In response, Applicants respectfully traverse.

These rejections are improper because Igusa et al. cannot be used to preclude patentability under 35 U.S.C. 103(c). Igusa et al. is a 102(e) reference, and the present application and Igusa et al. have common assignee at the time of the invention of the present application.

102(e) Reference

The present application has a priority filing date of May 14, 2004. The Igusa et al. reference was filed on August 12, 2002 and was patented on August 24, 2004. Therefore, Igusa et al. is a 102(e) reference with respect to the present application. In addition, Igusa (please double-check) does not qualify as a 102(a), (b), (c) or (d) reference.

Common Ownership

The present application and Igusa et al. were, at the time the invention of the present application was made, owned by Cadence Design System, Inc. (see MPEP 7706.02(l)(2)).

Therefore, Igusa et al. cannot be used to preclude patentability under 35 U.S.C. 103(c). (see MPEP 706.02(l)(3)). For at least the above reasons, Applicants request that the 35 U.S.C. 103(a) rejections for claims 18-20 be withdrawn.

CONCLUSION

Based on the foregoing, all remaining claims are in condition for allowance, which is respectfully requested. If the Examiner has any questions or comments regarding this response, the Examiner is respectfully requested to contact the undersigned at the number listed below.

To the extent that any arguments and disclaimers were presented to distinguish prior art, or for other reasons substantially related to patentability, during the prosecution of any and all parent and related application(s)/patent(s), Applicant(s) hereby explicitly retracts and rescinds any and all such arguments and disclaimers, and respectfully requests that the Examiner re-visit the prior art that such arguments and disclaimers were made to avoid.

The Commissioner is authorized to charge Vista IP Law Group LLP Account No. 50-1105 for any fees required that are not covered, in whole or in part, and to credit any overpayments to said Deposit Account No. 50-1105.

Respectfully submitted,

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